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MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA

Automated Workflow for Comprehensive Thermal Analysis of IC Package Designs

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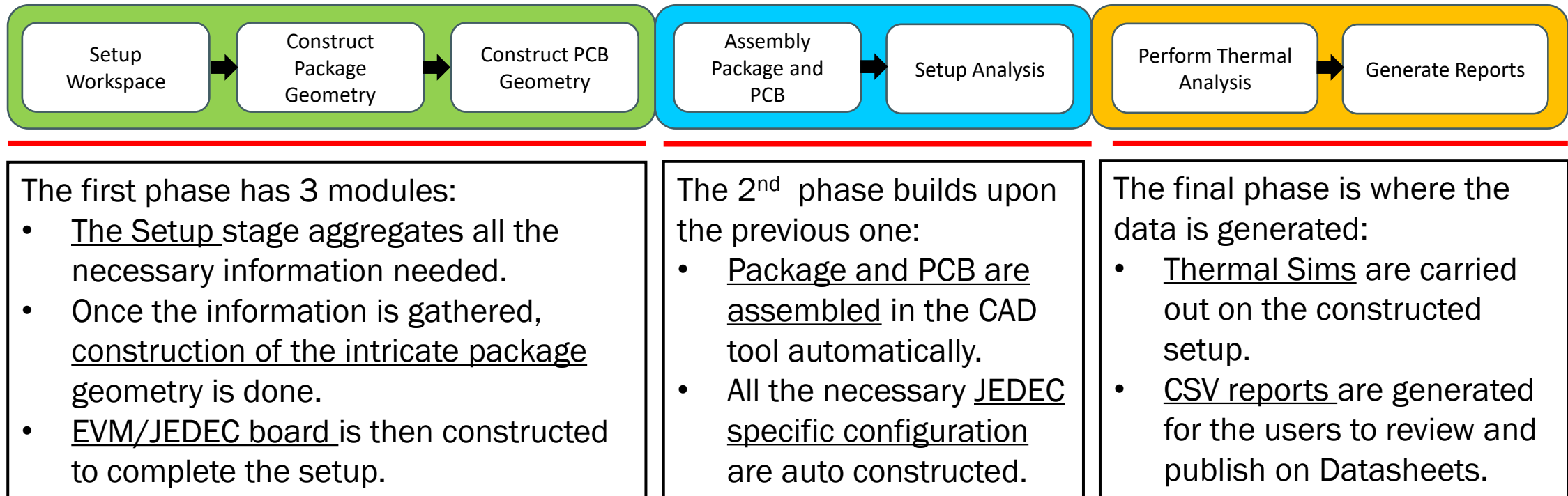


Motivation and Problem Statement

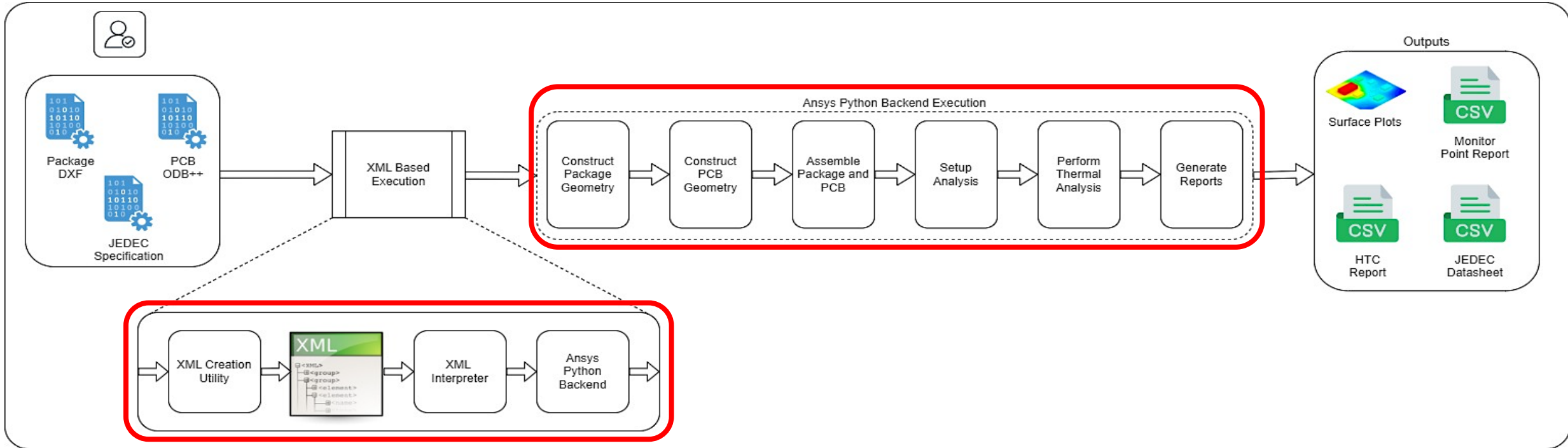
- TI products use a wide range of Packaging Technologies. In order to perform Thermal Modeling and Analysis, design teams need to spend significant time in ramping up on thermal modelling tools and also gather all critical information necessary which vary with each package family.
- Thermal Modeling requires manual creation of intricate Package Geometries along with a supporting PCB and simulation setup in CAD tools. This is both time consuming and error prone.
- In addition, Thermal Modeling consists of multiple iterations between design teams and Centralized Modeling team which can take upwards of 2+ weeks to complete.
- An automated solution will reduce the time taken for this iterative process of Thermal Modeling **from 2+ weeks to ~2 days**.
- Automation empowers design teams to independently perform Thermal Modeling without the need for extensive familiarity with CAD/Modeling tools or relying on expertise of the Centralized Modeling teams.
- The JEDEC datasheet values such as **Theta-JA** (θ_{JA}), **Theta-JC** (θ_{JC}), **Theta-JB** (θ_{JB}), **Psi-JB** (φ_{JB}) & **Psi-JT** (φ_{JT}) can also be automatically generated

Self Service Workflow – Overview

- The Framework is designed to address the challenges that design teams face during Thermal Analysis. Construction of Package, PCB, Thermal Chamber along with JEDEC specified setup are completely automated and is done using Ansys Icepak – Iron Python Scripting.
- The flow is strategically broken down into function based modules to increase usability.



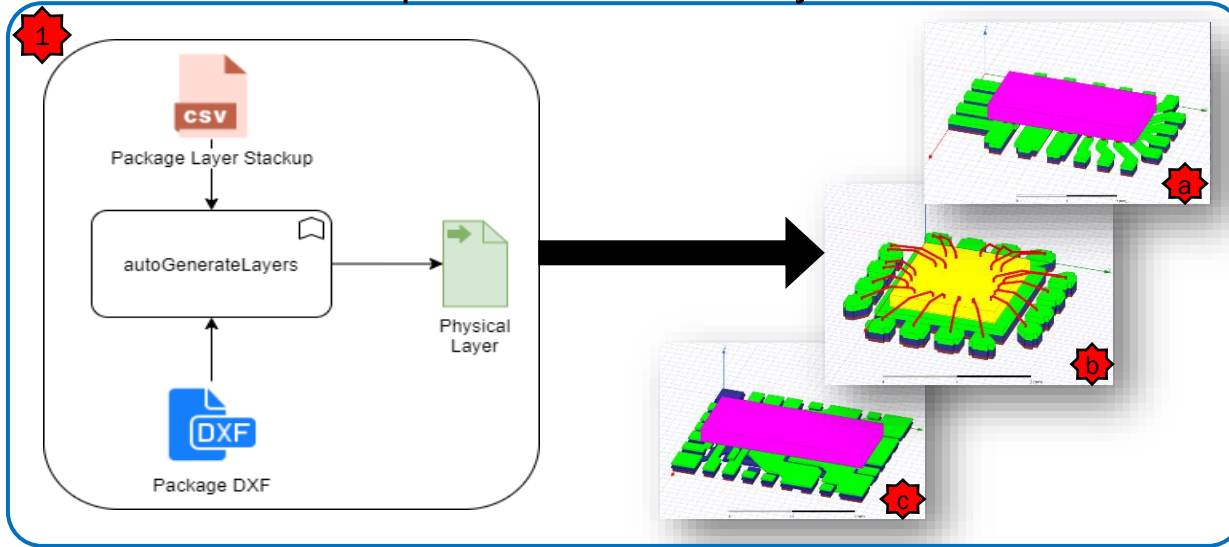
Overview of Flow Execution Steps



- One of the biggest challenge was to build an automation flow that was tool agnostic and would seamlessly integrate with any other vendor tool that we may end up using in the future.
- This is accomplished using an XML based framework and a custom XML interpreter that is able to parse the XML like an instruction set and issue commands via API calls to the vendor tool.
- The users' inputs are translated and combined into a XML file required for running the flow.
- The XML execution takes over the control from here and performs all the background tasks in Ansys Environment.

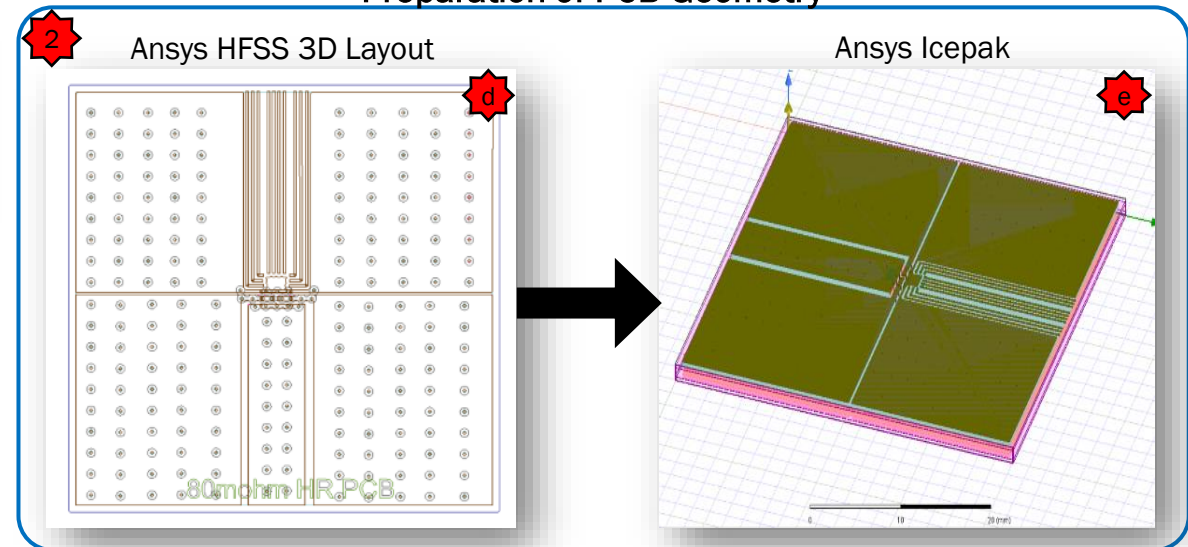
Outline of the Flow Steps / Modules

Preparation of PKG Geometry



- The intricate package geometry is automatically constructed based on the package_layer_stackup.csv file and the package DXF File.
- The stackup file contains all the details required to construct a given layer.
- Package DXF file is put through de-embedding step to make sure any holes present in the DXF are captured correctly and overlaps are merged to form a single continuous layer

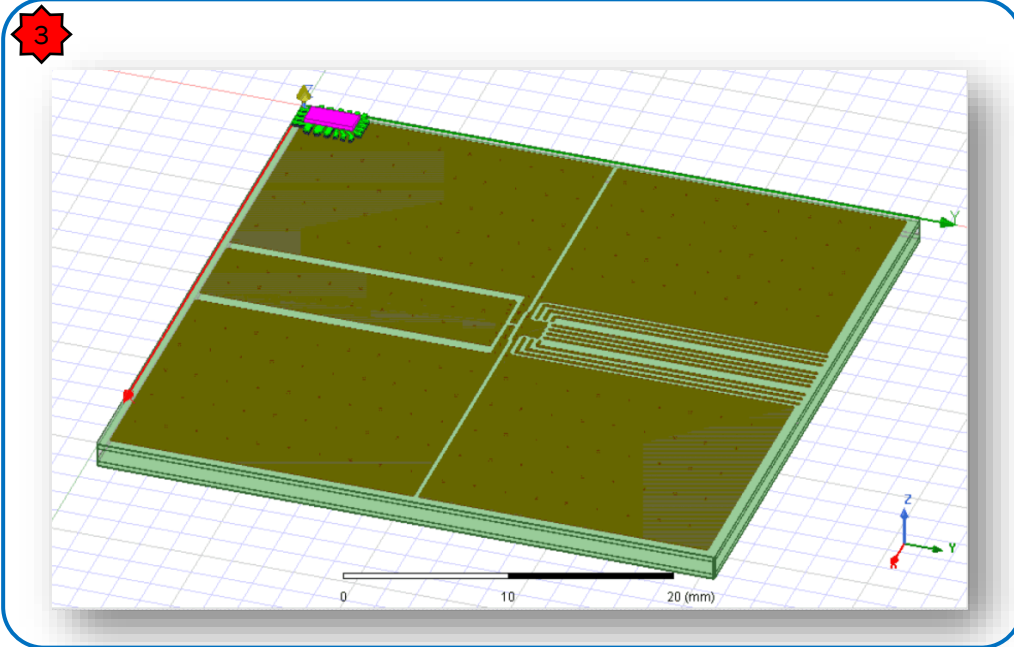
Preparation of PCB Geometry



- Here the PCB structure is constructed inside the Ansys Icepak environment using ODB++ file
- Using the layer material data available from the ODB++ files, the required materials are added in the material stack in AEDT*.
- The advantage of creating PCB in this way is that all the details represent within the PCB, down to the minute and complex geometric shapes can be translated without compromising the accuracy.

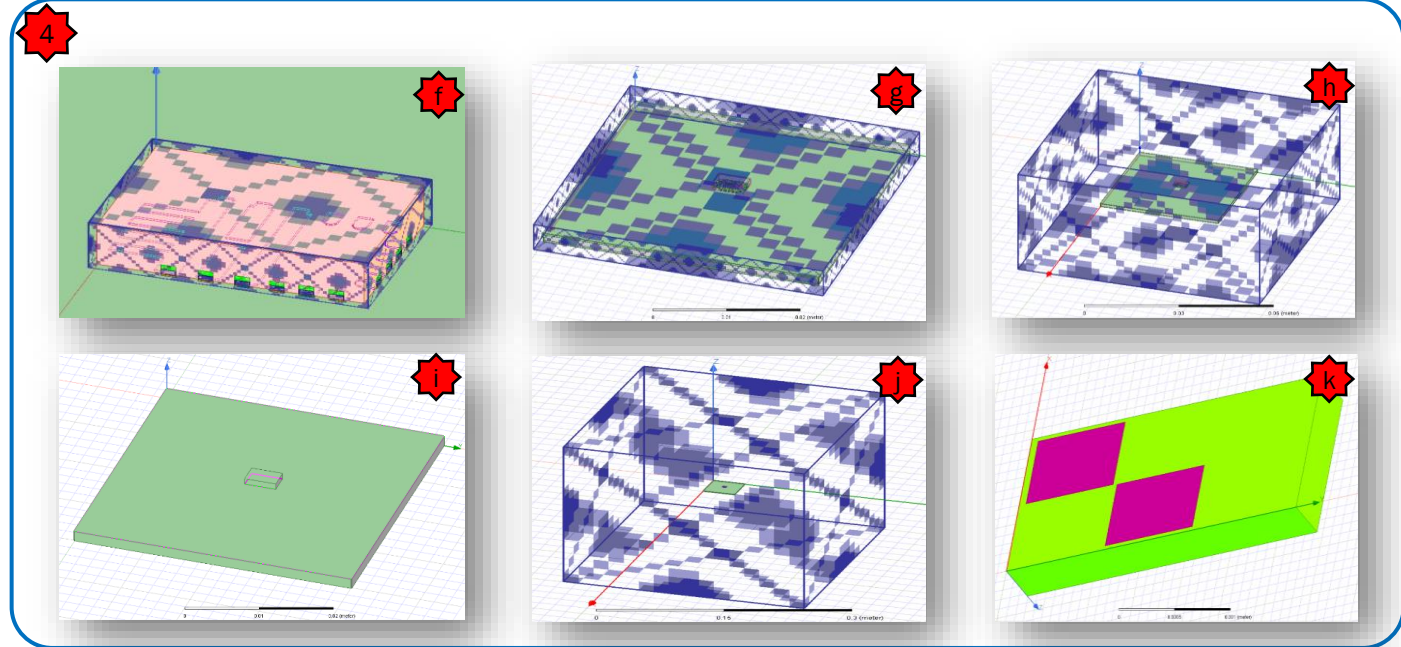
Outline of the Flow Steps / Modules

Assemble Package and PCB



- Once the Package and PCB are constructed, they have to be assembled.
- Ansys Icepak allows movement of all objects associated with a Coordinate System (CS) when CS is moved.
- This is used to move the entire package to the correct location on the PCB.

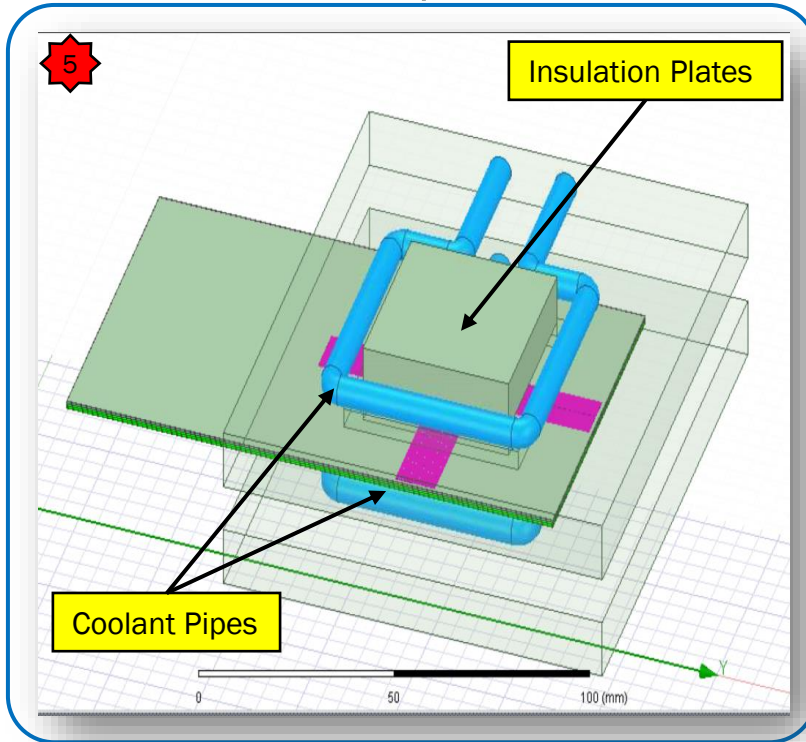
Mesh Generation and Analysis Setup



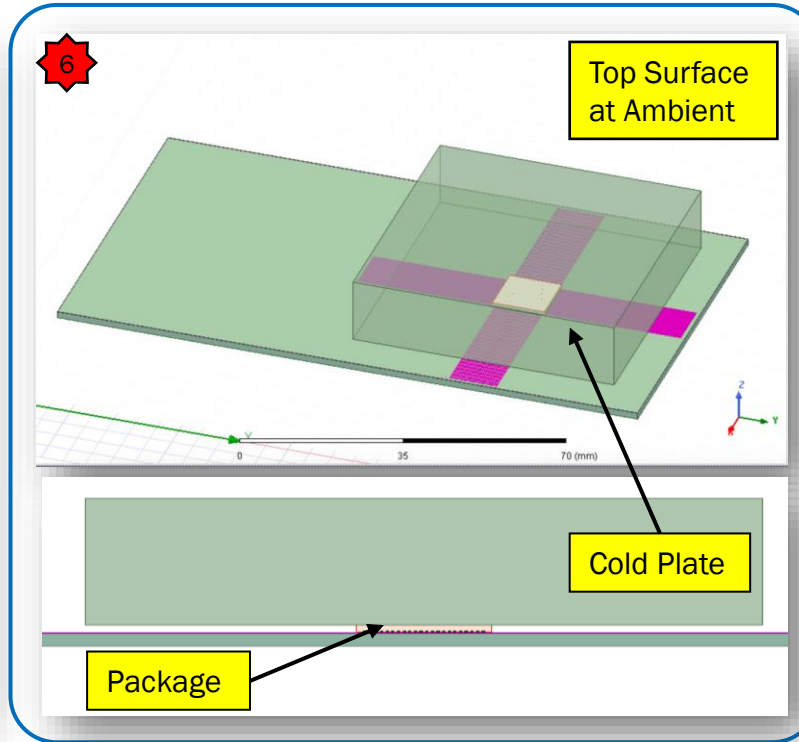
- Cascading set of meshes are created to mesh different regions of the setup appropriately [f, g, h]. This is crucial to maintain good meshing while not blowing up the meshing elements.
- HTC extraction planes around the PKG & PCB along with Stationary Wall around the setup is created. [i, j]
- Heat source pads are generated on the DIE surface to emulate the dissipated power from FETs. [k]

Outline of the Flow Steps / Modules

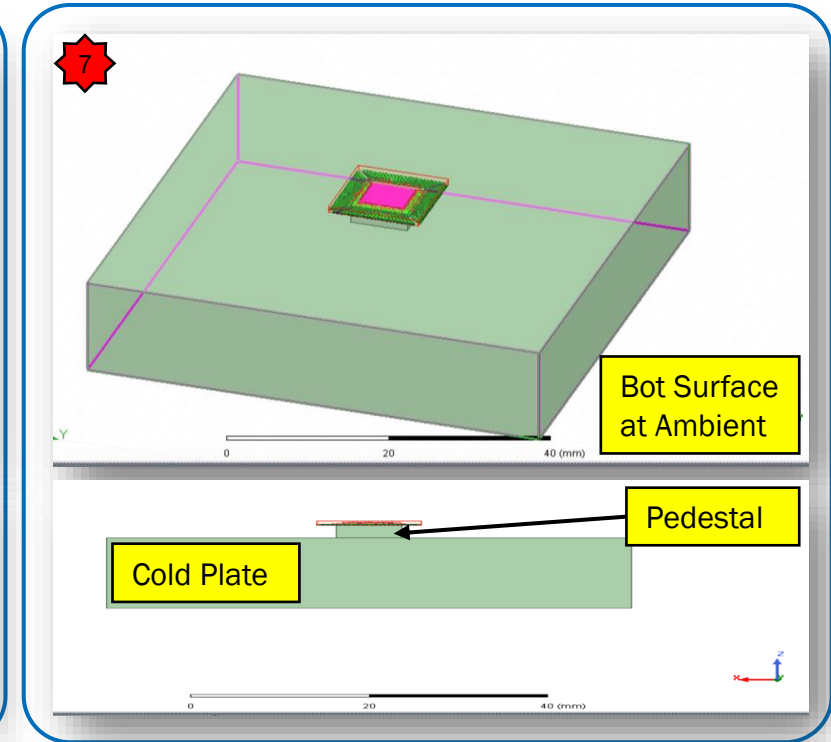
Theta-JB Setup Creation



Theta-JC Top Setup Creation



Theta-JC Bot Setup Creation

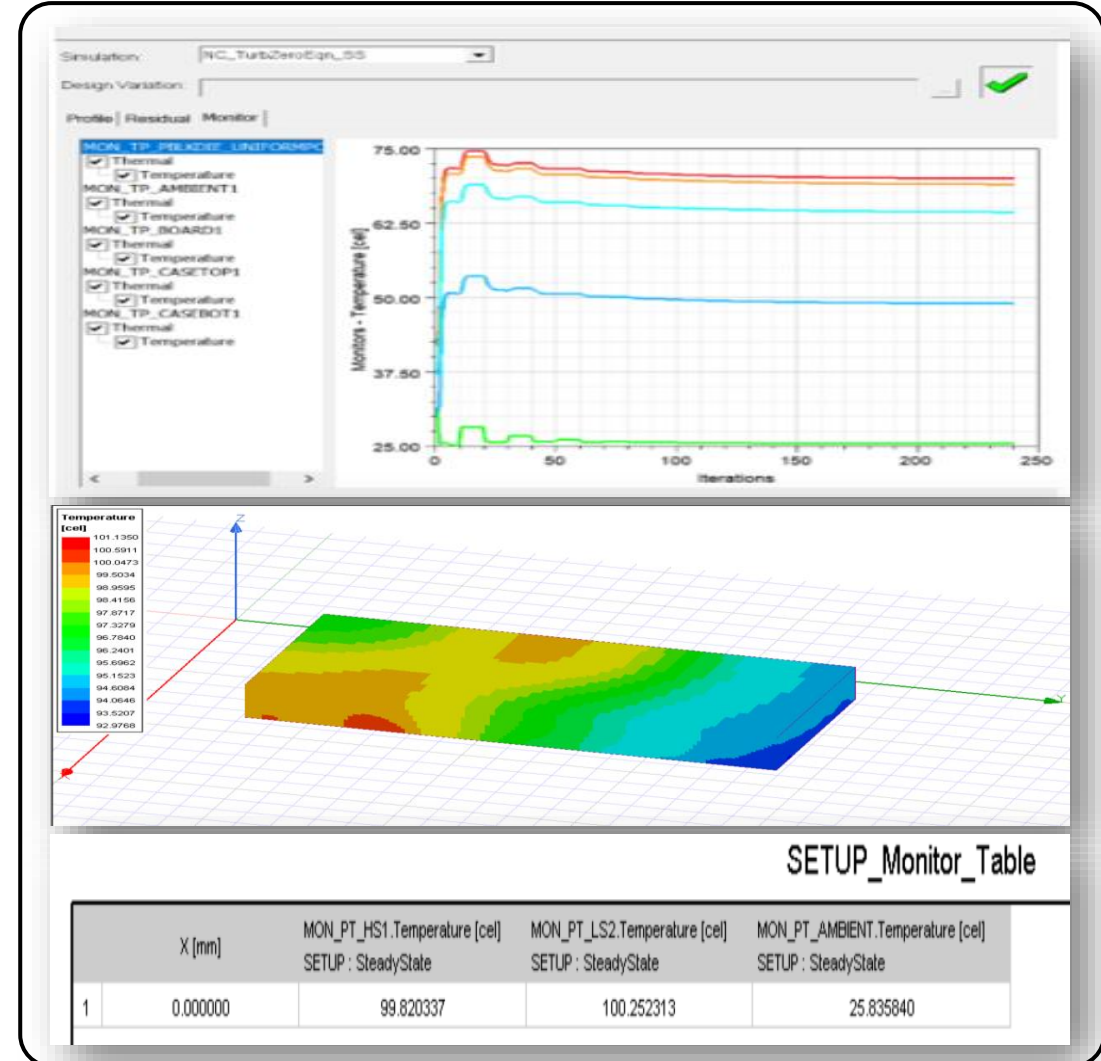


- Junction-to-Board (Theta-JB) thermal resistance sim environment needed to calculate θ_{JB} is constructed automatically using the specification from JEDEC Std # 51-8.
- Junction-to-Case (Theta-JC) which indicates the ease of heat flow between the Die junction and Package Top is calculated using another specific configuration, which is again constructed automatically following JEDEC standards.
- Two variants of Theta-JC require different setups. These are generated automatically as part of the JEDEC setup.

Outline of the Flow Steps / Modules

- Once all the setup is generated, Thermal Simulations are carried out in this step.
- Few design, based on the size of the Package and PCB, require a good memory machine to run the Thermal Simulations. The option to use a suitable machine which user needs can be provided as an input to the flow.
- Temperature Readouts via the Monitor window is shown while the simulation is happening.
- Once the simulation is done, the generate reports step presents the simulation data in a user friendly way.
- DIE Surface temperature plots along with HTC and JEDEC CSV reports are automatically generated.

Simulation and Temperature Contours



Results correlation with Manual Workflow

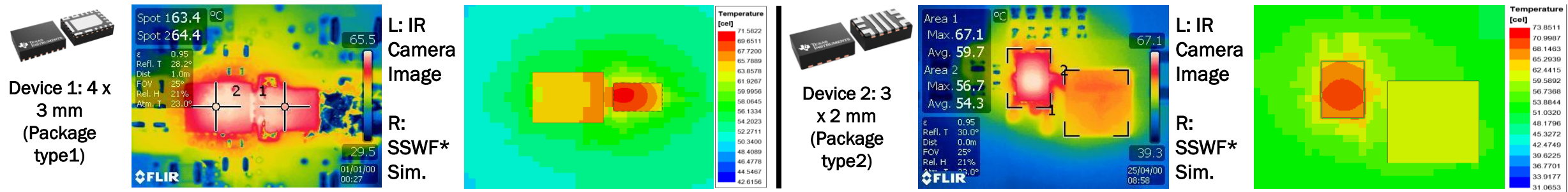
Design Name**	Pin Count	Max Die Temp (°C)		Max Case Temp (°C)		Theta-JA (°C/W)		Theta-JB (°C/W)		Theta-JC (Top) (°C/W)		Theta-JC (Bottom) (°C/W)		Psi-JT (°C/W)		Psi-JB (°C/W)	
		SSWF*	Manual	SSWF*	Manual	SSWF*	Manual	SSWF*	Manual	SSWF*	Manual	SSWF*	Manual	SSWF*	Manual	SSWF*	Manual
Design 1	6	103.9	102.5	98.94	97.6	78.53	74.2	42.52	39.5	90.78	89	17.51	14.4	5.01	3.2	45.81	39.5
Design 2	10	68.85	69.2	67.37	68.34	43.11	46.7	15.5	17.6	45.98	48.7	7.11	6.2	1.5	1	16.85	17.6
Design 3	24	57.31	57.4	57.12	57.23	31.73	31.9	9.16	9.6	24.1	26	2.65	2.8	0.32	0.3	9.9	9.6
Design 4	36	57.56	58.78	57.15	58.12	32.24	32.9	12.99	13.7	20.9	23.1	3.74	3.5	0.41	0.3	14.24	13.7
Design 5	64	45.51	45.32	45.41	45.18	20.11	20.2	7.18	5.3	6.5	7	0.58	0.56	0.1	0.1	5.06	5.2

- All cases assumed FR4 with $k=0.3$ W/m-K, 20 μ m DIE ATTACH, and even Power on DIE surface.
- All cases use JEDEC standard board. (The JEDEC board themselves are also automatically generated)
- All results obtained through automated workflow (SSWF) are within expected tolerance levels of the reference results obtained from manual workflow created using FloTherm***.

Empirical Data Correlation and Summary

- Validated SSWF simulations against thermal measurement data provided by internal Power BU.
- Good correlation between measurements and simulations, validating simulation approach accuracy

Parameter	Design 1 - Package 1	Design 2 - Package 2
Use Case	5V → 0.875V, 20A	5V → 1.8V, 4 A
Measured Temp.	65.5 °C	67.1 °C
Simulation Case Temp. obtained through SSWF*	70.5 °C	70.3 °C



Summary and Highlights:

- The solution drastically reduces time taken for Thermal Modeling of Packages from 2+ weeks to 2 days. Thereby providing significant improvement for TTM of the product.
- All groups in the Power domain in the company have seen significant benefit from the tool.
- First of its kind in the company to fully automate Thermal Modeling with PCB integration and Thermal Chamber setup.
- Currently seeing on average 800 to 1000 tool invocations per month by ~20 unique teams across the company.